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EXAMINER	
YAARY, MICHAEL D	
ART UNIT	**PAPER NUMBER**
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/693,344	KHAN ET AL.	
	Examiner	Art Unit	
	Michael Yaary	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *10/24/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/06/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. Claims 1-35 are pending in the application.

Claim Objections

2. Claim 22 recites the limitation "the first circuitry" in claim 22, line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 18-21 are rejected under U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. As provided in [0044], lines 6-10 of the specification, machine-readable medium may include...electrical, optical, acoustical or other form of propagated signals. Claims drawn to components involving signals encoded with functional descriptive material do not fall within any of the categories of statutory subject matter as set forth in 35 U.S.C. 101, and are therefore ineligible for protection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 22, 24-27, 29-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Asami et al. (hereafter Asami)(US Pub 2003/0014643).

Regarding claim 22, Asami discloses an apparatus, comprising:

A processor to execute instructions in a debug mode ([0034] lines 7-9);

Circuitry to contain control bits (Inherent in the circuitry of [0035], lines 1-8 as using control bits is the low level execution part of the permission analysis in the debugging system.); and

Circuitry coupled to the processor and to the first circuitry to determine a level of debug access permitted in the apparatus based on a state of the control bits ([0034], lines 1-17 and [0036], lines 1-8).

Regarding claim 27, Asami discloses a system, comprising:

A processor to execute instructions in a debug mode ([0034] lines 7-9);

A volatile memory coupled to the processor (RAM 21 of figure 1);

Circuitry to contain a set of control bits to indicate a level of debug access permitted during the debug mode based on a state of at least one of the control bits

([0034], lines 1-17; [0036], lines 1-8; and inherent in the circuitry of [0035], lines 1-8 as using control bits is the low level execution part of the permission analysis in the debugging system.); and

Circuitry to determine if the execution violates restrictions defined by the level of debug access ([0034], lines 1-5).

Regarding claim 32, Asami discloses a method, comprising:

Determining based on a set of control bits (Inherent in the circuitry of [0035], lines 1-8 as using control bits is the low level execution part of the permission analysis in the debugging system.), a current level of authorized debug access ([0034], lines 1-17 and [0036], lines 1-8);

Executing at least one instruction in a trusted subsystem in a debug mode of operation ([0034], lines 1-5); and

Not presenting a result of said executing if said executing violates restrictions defined by the current level of authorized debug access ([0034], lines 9-13).

Regarding claim 24, Asami discloses an interface coupled to the processor to provide said debug access ([0019], lines 1-3).

Regarding claim 25 and 35, Asami discloses wherein said circuitry to determine a level of debug access is to determine restrictions for at least one of:

An address range within which said at least one instruction may be located ([0034], lines 1-5).

Regarding claim 26, Asami discloses to abort the debug access resultant to said debug access violating at least one of said restrictions ([0036], lines 1-5).

Regarding claim 29, Asami discloses to present a result of the execution to a debug interface if the execution does not violate the restrictions ([0034], lines 1-5) and to not present the result of the execution to the debug interface if the execution violates the restrictions ([0034], lines 9-13).

Regarding claim 30 and 33, Asami discloses to abort the debug mode if the execution violates the restriction ([0036], lines 1-5).

Regarding claim 31, Asami discloses the circuitry to determine if the execution violates the restrictions is adapted to make said determination after execution of a predetermined group of at least one instruction ([0034], lines 1-5).

Regarding claim 34, Asami discloses presenting the result of said executing if said executing does not violate the restrictions defined by the current level of debug access ([0034], lines 6-9).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3, 6-10, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asami in view of Bouchier et al. (hereafter Bouchier)(US Pat. 6,684,343).

Regarding claim 1, Asami discloses an apparatus comprising:

A first circuitry to permit access to a first set of resources to debug a first set of code in memory ([0026], lines 5-9);

A storage structure ([0038], lines 1-3); and

A second circuitry coupled to the first circuitry and to the storage structure to permit access to a second set of resources to debug a second set of code in the memory ([0006], lines 1-10 and [0017], lines 1-11 disclose security measures needed to prevent third party access to LSIs (circuits) when debugging.).

Asami does not disclose the first circuitry being responsive to entering a first password and a second circuitry being responsive to entering a second password.

However, Bouchier discloses the first circuitry being responsive to entering a first password and a second circuitry being responsive to entering a second password (Column 9, lines 60-67 disclose a partition system in which a hierarchy of different levels are implemented in which different users have different passwords to limit access to areas only to authorized users, and prevent unauthorized users from obtaining access. Each partition user has a unique password to be used, thus reading on having the different circuitry being responsive to different passwords entered.)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Asami by, implementing a password incorporated security system as taught by Bouchier, for the benefit of only limiting access to authorized users (Bouchier column 9, lines 60-61).

Regarding claim 9, Asami discloses a system comprising:

A volatile first memory (RAM 21 of figure 1);

A second memory coupled to the first memory to contain code for execution (ROM 22 of figure 1);

A processor coupled to the second memory to execute the code (CPU 2-2 of figure 1); and

Circuitry to permit access to a first set of resources to debug a first set of code in the second memory, to disable said access to the first set of resources, and to debug a second set of code in the second memory ([0006], lines 1-10; [0017], lines 1-11; and [0026], lines 5-9 disclose security measures needed to prevent third party access to LSIs (circuits) when debugging. [0038], lines 3-12 disclose different permission levels being set preventing access to certain debug resources for different users, thus disabling access to resources to users who do not have permission to have access.)

Asami does not disclose a first and a second storage structure coupled to the processor to contain a first and second password, enabling access to a first set of resources in response to entering a first password, and enabling access to a second set of resources in response to entering a second password.

However, Bouchier discloses a first and a second storage structure coupled to the processor to contain a first and second password (Column 2, lines 21-25 disclose partitions each containing its own memory storage, thus able to store a password), enabling access to a first set of resources in response to entering a first password and enabling access to a second set of resources in response to entering a second password (Column 9, lines 60-67 disclose a partition system in which a hierarchy of

different levels are implemented in which different users have different passwords to limit access to areas only to authorized users, and prevent unauthorized users from obtaining access. Each partition user has a unique password to be used, thus reading on permitting access in response to different passwords being entered.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Asami by, implementing more than one storage and a password incorporated security system as taught by Bouchier, for the benefit of only limiting access to authorized users (Bouchier column 9, lines 60-61).

Regarding claim 18, Asami discloses a machine-readable medium that provides instructions which when executed by a computing platform (abstract), cause said computing platform to perform operations comprising:

Enable debug of a first set of code during a first debug stage ([0006], lines 1-10 and [0017], lines 1-11 disclose security measures needed to prevent third party access to LSIs (circuits) when debugging, thus debugging being done in multiple stages by different parties.);

Preventing further debugging activities during the first debug stage ([0038], lines 3-12 disclose different permission levels being set preventing access to certain debug resources for different users, thus disabling access to resources to users who do not have permission to have access and preventing the debug operations from occurring.); and

Enabling debug of a second set of code during a second debug stage ([0006], lines 1-10 and [0017], lines 1-11 disclose security measures needed to prevent third

party access to LSIs (circuits) when debugging, thus debugging being done in multiple stages by different parties.).

Asami does not disclose storing a second password and that the enabling and disabling are done by receiving a first password and receiving the second password.

However, Bouchier discloses storing a second password (Column 2, lines 21-25 disclose partitions each containing its own memory storage, thus able to store a password) and that the enabling and disabling are done by receiving a first password and receiving the second password (Column 9, lines 60-67 disclose a partition system in which a hierarchy of different levels are implemented in which different users have different passwords to limit access to areas only to authorized users, and preventing unauthorized users from obtaining access. Each partition user has a unique password to be used. The password system implemented in the system of Asami would allow for certain passwords to be disabled while others are allowed to be entered.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Asami by, storing a password and implementing a password incorporated security system as taught by Bouchier, for the benefit of only limiting access to authorized users (Bouchier column 9, lines 60-61).

Regarding claim 2 and 10, Asami further discloses the first and second access are to be through a debug interface ([0019], lines 1-3).

Regarding claim 3, Asami further discloses the second set of code is placed in a substantially different portion of the memory than the first set of code ([0017], lines 17-

20 disclose different sets of address ranges to be debugged, thus the codes are in different memory portions).

Regarding claim 6, Asami further discloses the storage structure comprises a programmable storage structure (flash memory 72 of figure 6).

Regarding claim 7, Asami further discloses said first set of resources comprises a first portion of the memory and said second set of resources comprises a second portion of the memory different than the first portion ([0017], lines 17-20).

Regarding claim 8, Asami further discloses the second set of resources is substantially a subset of the first set of resources ([0021], lines 7-10) and [0038], lines 1-6).

Regarding claim 19, Asami does not disclose the operation of disabling the first password prevents access to the first set of code during the second debug stage.

However, Bouchier discloses the operation of disabling the first password prevents access to the first set of code during the second debug stage (Column 9, lines 60-67 disclose a partition system in which a hierarchy of different levels are implemented in which different users have different passwords to limit access to areas only to authorized users, and preventing unauthorized users from obtaining access. This would prevent a user from having access in one debugging stage to a different set of code that the user does not have permission to access.)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Asami by preventing users from accessing areas in which they do not have permission to access, as taught by Bouchier,

for the benefit of only limiting access to areas, to users who are authorized (Bouchier column 9, lines 60-61).

8. Claims 23 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asami as applied to claim 22 and 27 above, and further in view of Moyer et al. (hereafter Moyer)(US Pub. 2003/0177373.

Regarding claim 23, Asami does not disclose circuitry to contain control bits comprises a set of programmable fuses.

However, Moyer discloses circuitry to contain control bits comprises a set of programmable fuses ([0014], lines 7-9 and [0020], lines 11-13 disclose using circuits such as programmable fuses in the system of preventing unauthorized access to an IC.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Asami by, implementing programmable fuses for providing security as taught by Moyer, in order to have a one-time programmable non-volatile storage circuit (Moyer, [0014], lines 7-8).

Regarding claim 28, Asami does not disclose the state of the control bits is non-alterable after manufacture of the circuitry.

However, Moyer discloses the state of the control bits is non-alterable after manufacture of the circuitry (Inherent in [0020], lines 11-13 as disclosed is one-time programmable storage circuit such as a programmable fuse, thus only being programmed and altered at the time of manufacture).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Asami by, implementing one-time programmable fuses for providing security as taught by Moyer, for the benefit of not having to deal with bit alterations at more the one time.

9. Claims 5, 12-17, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asami in view of Bouchier and further in view of Kelley et al. (hereafter Kelley)(US Pat. 6,000,033).

Regarding claim 5, Asami and Bouchier do not disclose circuitry to prevent the access responsive to said entering the first password if the access responsive to said entering the second password is enabled, and to prevent the access responsive to said entering the second password if the access responsive to said entering the first password is enabled.

However, Kelley discloses circuitry to prevent the access responsive to said entering the first password if the access responsive to said entering the second password is enabled, and to prevent the access responsive to said entering the second password if the access responsive to said entering the first password is enabled (Column 7, lines 40-44 disclose services authorized by passwords to be mutually exclusive, thus enabling the access to those different services to be mutually exclusive.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Asami and Bouchier by, including a system providing mutually exclusive access as taught by Kelley, for the benefit of providing a more secure and exclusive form of authorization access.

Regarding claim 12, Asami and Bouchier do not disclose the circuitry is adapted to cause the access responsive to said entering the first password and the access responsive to said entering the second password to be mutually exclusive.

However, Kelley discloses the circuitry is adapted to cause the access responsive to said entering the first password and the access responsive to said entering the second password to be mutually exclusive (Column 7, lines 40-44 disclose services authorized by passwords to be mutually exclusive, thus enabling the access to those different services to be mutually exclusive.)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Asami and Bouchier by, including a system providing mutually exclusive access as taught by Kelley, for the benefit of providing a more secure and exclusive form of authorization access.

Regarding claim 13, Asami discloses a method, comprising:

Disabling performing a first set of code debug operations ([0038], lines 3-12 disclose different permission levels being set preventing access to certain debug resources for different users, thus disabling access to resources to users who do not have permission to have access and preventing the debug operations from occurring.);

Enable performing a second set of code debug operations ([0006], lines 1-10 and [0017], lines 1-11 disclose security measures needed to prevent third party access to LSIs (circuits) when debugging, thus debugging being done in multiple stages by different parties.).

Asami does not disclose storing a second password and what is disabled is a first password and what is entered is a second password.

However, Bouchier discloses storing a second password (Column 2, lines 21-25 disclose partitions each containing its own memory storage, thus able to store a password) and that what is disabled is a first password and what is entered is a second password (Column 9, lines 60-67 disclose a partition system in which a hierarchy of different levels are implemented in which different users have different passwords to limit access to areas only to authorized users, and prevent unauthorized users from obtaining access. Each partition user has a unique password to be used. The password system implemented in the system of Asami would allow for certain passwords to be disabled while others allowed to be entered.)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Asami by, storing a password and implementing a password incorporated security system as taught by Bouchier, for the benefit of only limiting access to authorized users (Bouchier column 9, lines 60-61).

Asami and Bouchier do not disclose wherein being able to perform the first set of code debug operations and being enabled to perform the second set of code debug operations are mutually exclusive.

However, Kelley discloses wherein being able to perform the first set of code debug operations and being enabled to perform the second set of code debug operations are mutually exclusive (Column 7, lines 40-44 disclose services authorized by passwords to be mutually exclusive, thus enabling the access to those different services to be mutually exclusive.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Asami and Bouchier by, including a system providing mutually exclusive access as taught by Kelley, for the benefit of providing a more secure and exclusive form of authorization access.

Regarding claim 14, Asami further discloses being enabled to perform the second set of code debug operations comprises being enabled to perform a subset of the first code debug operations ([0038], lines 1-6).

Regarding claim 15, Asami further discloses said first and second code debug operations are performed through a debug interface ([0019], lines 1-3).

Regarding claims 16 and 20, Asami and Bouchier do not disclose said disabling the first password results from said storing the second password.

However, Kelley discloses said disabling the first password results from said storing the second password (Column 7, lines 40-44 disclose services authorized by passwords to be mutually exclusive, thus enabling the access to those different services to be mutually exclusive. Storing and implementing a second password in a mutually

exclusive environment would result in the disablement of the first password, as it would be unable to be used.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Asami and Bouchier by, including a system providing mutually exclusive access as taught by Kelley, for the benefit of providing a more secure form of authorization access.

Regarding claims 17 and 21, Asami and Bouchier do not disclose a third password that re-enables said performing of the first set of code debug operations.

However, Kelley discloses a third password that re-enables said performing of the first set of code debug operations (Column 7, lines 40-44 disclose services authorized by passwords to be mutually exclusive, thus enabling the access to those different services to be mutually exclusive. Enabling another password in a mutually exclusive environment would thus, disable a first password, and enable or re-enable another set of code to be debugged.)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Asami and Bouchier by, including a system providing mutually exclusive access as taught by Kelley, for the benefit of providing a more secure form of authorization access.

10. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asami and Bouchier as applied to claims 1 and 9 above, and further in view of Gwilt et al. (hereafter Gwilt)(US Pat. 6,532,553).

Regarding claims 4 and 11, Asami and Bouchier do not disclose the storage structure comprises a content addressable memory.

However, Gwilt discloses the storage structure comprises a content addressable memory (Column 3, lines 62-66 disclose a CAM used in a debugging system).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Asami and Bouchier by, including a CAM in the debugging system and apparatus as taught by Gwilt, for the benefit of utilizing a much faster memory with regards to searching through the storage.

Conclusions

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Yaary whose telephone number is (571) 270-1249. The examiner can normally be reached on Monday-Friday, 8:00 a.m - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nabil El-Hady can be reached on (571) 272-3963. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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